

MITSUBISHI LSIs M58725P, -15

16 384-BIT (2048-WORD BY 8-BIT) STATIC RAM

DESCRIPTION

This is a family of 2048-word by 8-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. These devices operate on a single 5V supply, as does TTL, and are directly TTL-compatible.

The input and output terminals are common, and an \overline{OE} terminal is provided. \overline{S} controls the power-down feature.

FEATURES

- Fast access time:

M58725P	200ns (max)
M58725 P-15	150ns (max)
- Low power dissipation:

Active:	250mW (typ)
Stand by:	25mW (typ)
- Power down by \overline{S}
- Single 5V supply voltage ($\pm 10\%$ tolerance)
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- All outputs are three-state, with OR-tie capability
- Easy memory expansion by chip-select (\overline{S}) input
- Common data DQ terminals.
- Same pin configuration as M5L2716K 16 384-bit EPROM

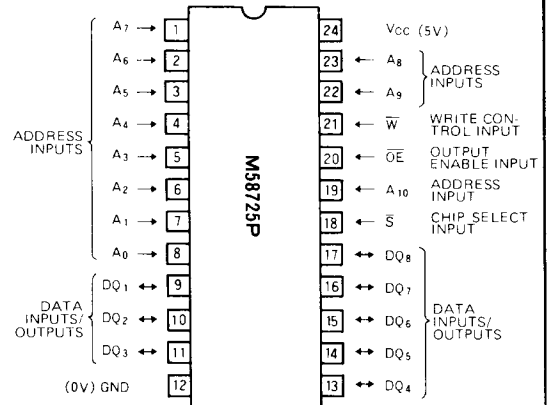
APPLICATION

- Small-capacity memory units

FUNCTION

These devices provide common data input and output terminals. During a write cycle, when a location is designated by address signals $A_0 \sim A_{10}$ the \overline{OE} signal is kept high to keep the DQ terminals in the input mode, signal \overline{W} goes low, and the data of the DQ signal at that time is written.

PIN CONFIGURATION (TOP VIEW)



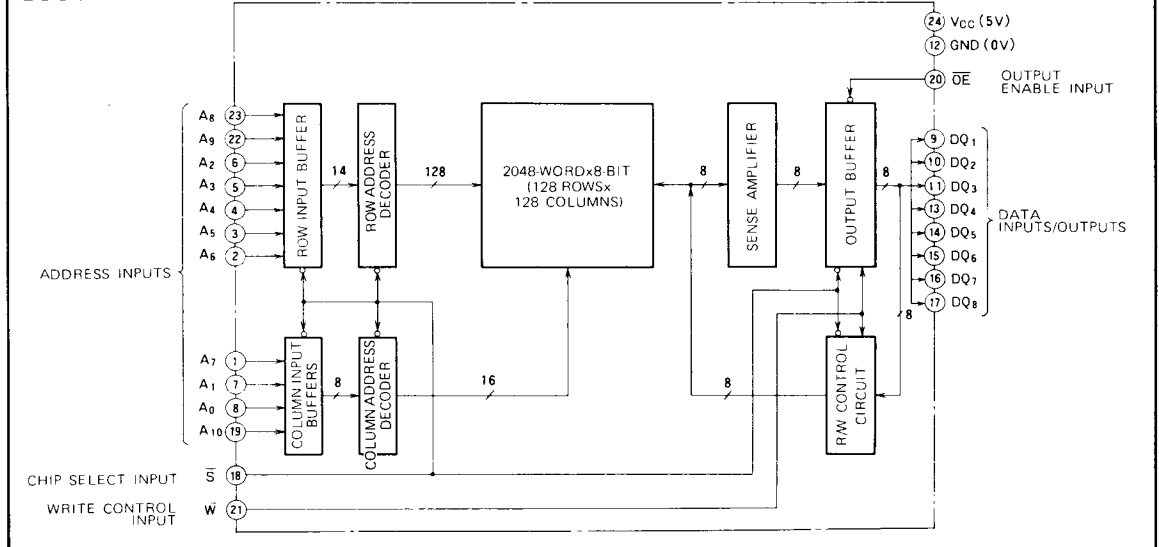
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During a read cycle, when a location is designated by address signals $A_0 \sim A_{10}$ the \overline{OE} signal is kept low to keep the DQ terminals in the output mode, signal \overline{W} goes high, and the data of the designated address is available at the I/O terminals.

When signal \overline{S} is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

Signal \overline{S} controls the power down feature. When \overline{S} goes high power dissipation is reduced to 1/10 of active power. The access time from \overline{S} is equivalent to the address access time.

BLOCK DIAGRAM



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FUNCTION TABLE

\overline{S}	\overline{OE}	\overline{W}	DQ ₁ ~DQ ₈	Mode
H	X	X	Hi-Z	Deselect
L	X	L	D _{IN}	Write
L	L	H	D _{OUT}	Read
L	H	H	Hi-Z	—

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Limits	Unit
V _{CC}	Supply voltage	With respect to GND	-0.5 ~ 7	V
V _I	Input voltage		-0.5 ~ 7	V
V _O	Output voltage		-0.5 ~ 7	V
P _d	Maximum power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating free-air ambient temperature range		0 ~ 70	°C
T _{stg}	Storage temperature range		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IL}	Low-level input voltage	-1		0.8	V
V _{IH}	High-level input voltage	2		6	V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2		6	V
V _{IL}	Low-level input voltage		-1		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -1mA, V _{CC} = 4.5V	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 3.2mA			0.4	V
I _I	Input current	V _I = 0 ~ 5.5V			10	μA
I _{OZH}	Off-state high-level output current	V _I (\overline{S}) = 2V, V _O = 2.4V ~ V _{CC}			10	μA
I _{OZL}	Off-state low-level output current	V _I (\overline{S}) = 2V, V _O = 0.4V			-10	μA
I _{CC1}	Supply current from V _{CC}	V _I = 5.5V, V _I (\overline{S}) = 0.8V, outputs open	T _a = 25°C	50	80	mA
			T _a = 0°C		90	mA
I _{CC2}	Stand by current	V _I = 5.5V, V _I (\overline{S}) = 2V, outputs open	T _a = 25°C	5	10	mA
			T _a = 70°C	7	15	mA
C _I	Input capacitance, all inputs	V _I = GND, V _i = 25mVrms, f = 1MHz		3	5	pF
C _O	Output capacitance	V _O = GND, V _o = 25mVrms, f = 1MHz		5	8	pF

Note 1: Current flowing into an IC is positive, out is negative.

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SWITCHING CHARACTERISTICS (For Read Cycle) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

Symbol	Parameter	M58725P-15			M58725P			Unit
		Limits						
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	150			200			ns
$t_a (A)$	Address access time			150			200	ns
$t_a (\bar{S})$	Chip select access time			150			200	ns
$t_a (\bar{OE})$	Output enable access time			50			60	ns
$t_v (A)$	Data valid time after address	20			20			ns
$t_{PXZ} (\bar{S})$	Output disable time after chip select			50			60	ns
$t_{PXZ} (\bar{S})$	Output active time after chip select	10			20			ns
t_{PU}	Power up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			60			80	ns

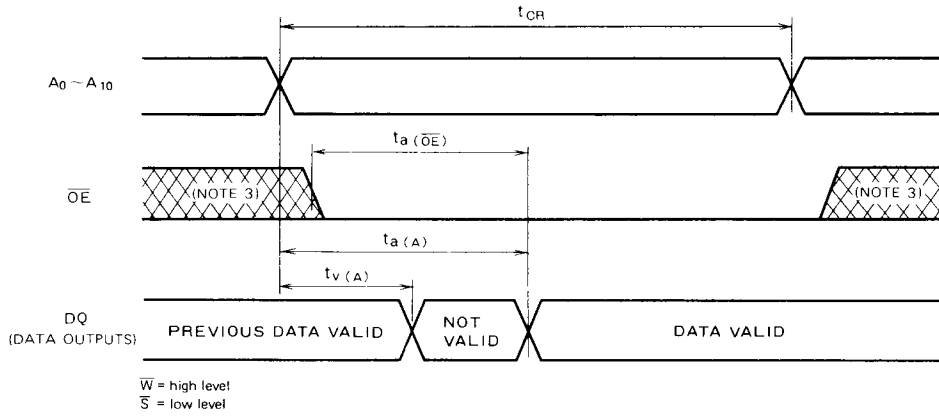
TIMING REQUIREMENTS (For Write Cycle) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

Symbol	Parameter	M58725P-15			M58725P			Unit
		Limits						
		Min	Typ	Max	Min	Typ	Max	
t_{OW}	Write cycle time	150			200			ns
$t_{su} (\bar{S})$	Chip select setup time	100			120			ns
$t_{su} (A)$	Address setup time	20			20			ns
$t_w (\bar{W})$	Write pulse width	80			100			ns
t_{wr}	Write recovery time	10			10			ns
$t_{su} (\bar{OE})$	Output enable setup time	40			40			ns
$t_{su} (D)$	Data setup time	60			60			ns
$t_h (D)$	Data hold time	10			10			ns
$t_{PXZ} (\bar{OE})$	Output disable time after output enable			40			40	ns
$t_{PXZ} (\bar{W})$	Output disable time after write enable			40			40	ns

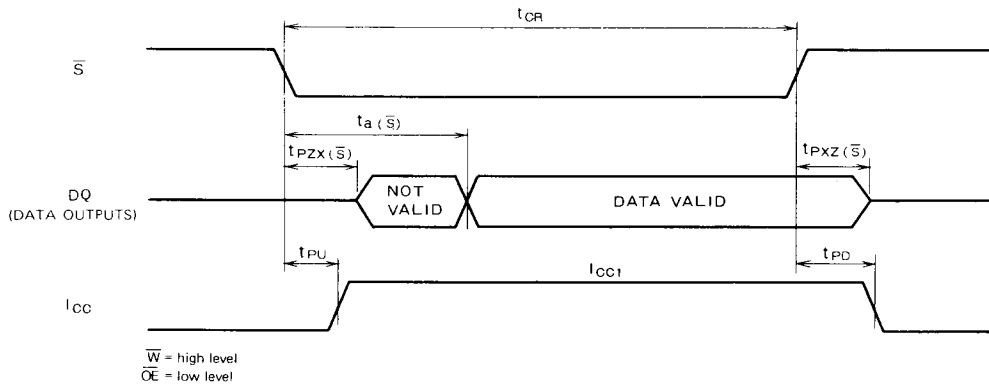
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TIMING DIAGRAMS (Note 2)

Read Cycle 1

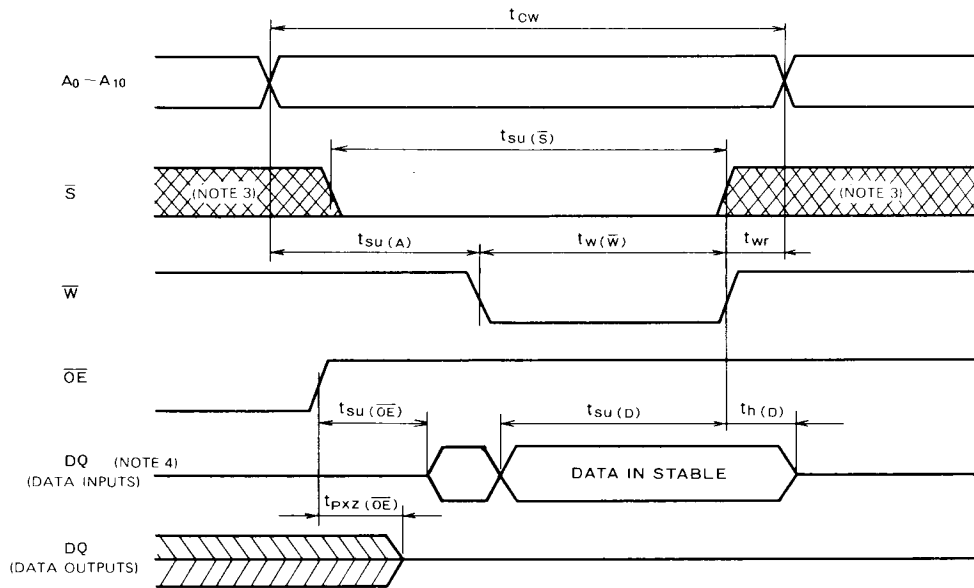


Read Cycle 2

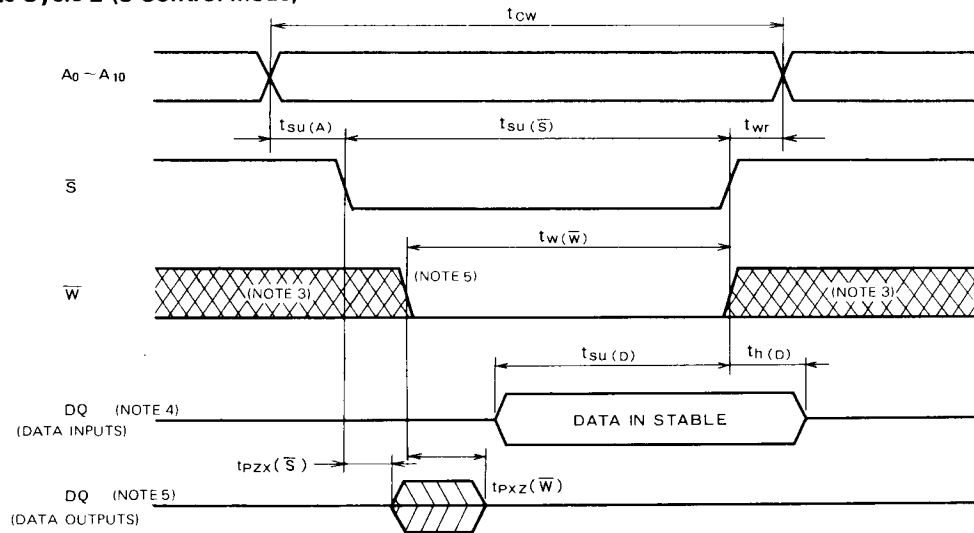


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Write Cycle 1 (\overline{W} Control Mode)



Write Cycle 2 (\overline{S} Control Mode)



\overline{OE} = low level

Note 2. Test conditions

Input pulse level	0.4 ~ 2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level	1.5V
Load	1TTL, $C_L = 100pF$

Note 3. Either the high or low state is possible.

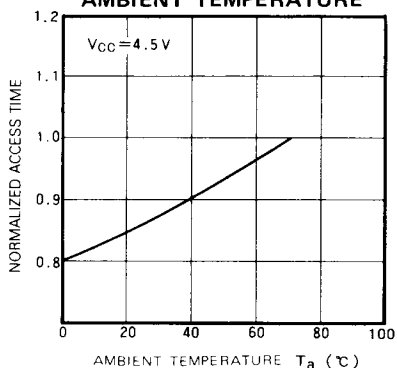
4. When the DQ pin is in the output state, a reverse phase signal should not be applied externally.

5. When the falling edge of \overline{W} is simultaneous to or prior to the falling edge of \overline{S} , the output is maintained in the high-impedance state.

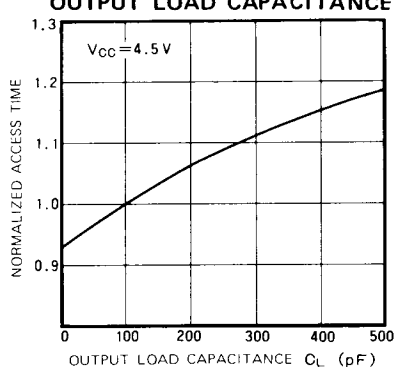
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TYPICAL CHARACTERISTICS

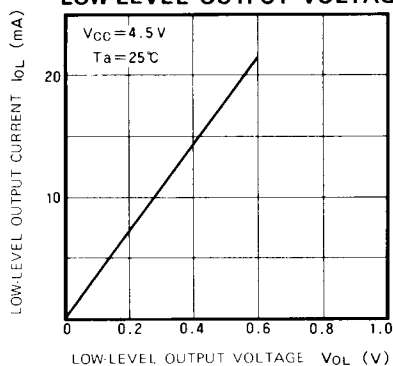
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



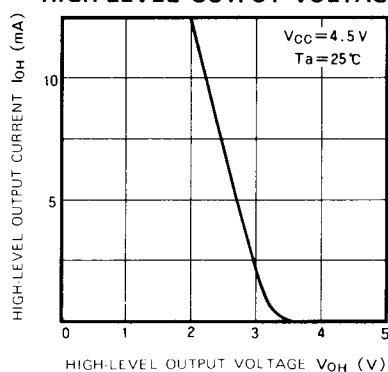
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



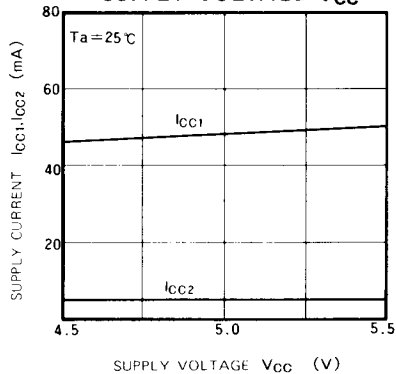
LOW-LEVEL OUTPUT CURRENT VS. LOW-LEVEL OUTPUT VOLTAGE



HIGH-LEVEL OUTPUT CURRENT VS. HIGH-LEVEL OUTPUT VOLTAGE



SUPPLY CURRENT VS. SUPPLY VOLTAGE V_{CC}



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

